

IN THE CLAIMS:

Please amend claims 1, 2, 4 and 5 as follows, and add claim 6:

1. (Currently Amended) A hybrid tester architecture for testing and repairing a plurality of semiconductor devices in parallel, each semiconductor device having a predetermined number of pins, the hybrid tester architecture including:
a computer workstation;
5 ~~per pin formatting circuitry~~ a plurality of formatting circuits, each
having data input circuitry and clock input circuitry, the plurality of formatting circuits
adapted for a one-to-one correspondence with each pin of each semiconductor device;
shared timing ~~circuitry~~ circuits coupled to the clock input circuitry,
each of the shared timing ~~circuitry~~ circuits operative to generate programmed timing
10 signals and adapted for coupling to more than one pin of the semiconductor devices;
and
~~per pin~~ a plurality of data ~~circuitry~~ circuits coupled to the data input
circuitry, each of the per pin ~~plurality of data circuitry~~ circuits adapted for a one-to-one
correspondence with each pin of each semiconductor device and operative to generate
15 drive data associated with each individual device pin;
—whereby the ~~per pin formatting circuitry~~ is responsive to the
programmed timing signals to generate tester waveforms in accordance with the ~~per~~
~~pin data.~~

20 2. (Currently Amended) A hybrid tester architecture according to claim 1
wherein:
the ~~per pin~~ plurality of data ~~circuitry~~ circuits comprises a plurality of
memory blocks, each memory block corresponding to one of the predetermined
number of pins.

25 3. (Original) A hybrid tester architecture according to claim 1 and further
including:
a capture memory for storing fail data relating to the plurality of
semiconductor devices; and
5 redundancy analyzer circuitry for processing the failure
data into a repair solution.

4. (Currently Amended) A hybrid tester architecture according to claim 3 and further including a computer workstation and wherein the redundancy analyzer is coupled to the computer workstation and operative, after generating repair solutions, to transmit the repair solutions to the computer workstation.

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5. (Currently Amended) A method of testing a plurality of semiconductor devices, each of the devices having a plurality of pins and redundant row and column addresses, the method including the steps:

generating test data signals unique to each of the plurality of pins;
5 clocking the ~~unique~~ test data signals through unique formatting
circuitry with shared timing signals;
applying the test data signals to the plurality of semiconductor devices;
detecting and storing failure data relating to the plurality of
semiconductor devices;
10 analyzing the failure data to generate repair solutions for activating
~~certain of the redundant rows and columns for each of the plurality of semiconductor~~
~~devices;~~
~~—— routing the repair solutions back to the computer workstation; and~~
~~—— programming the plurality of semiconductor devices to activate the~~
15 ~~desired redundant rows and columns based on the repair solutions.~~

6. (New) A hybrid tester architecture for testing and repairing a plurality of semiconductor devices in parallel, each semiconductor device having a predetermined number of pins, the hybrid tester architecture including:

means for generating test data unique to each of the plurality of pins;
5 means for clocking the unique test data through unique formatting
circuitry with shared timing signals;
means for applying the test signals to the plurality of semiconductor
devices;
means for detecting and storing failure data relating to the plurality of
10 semiconductor devices; and
means for analyzing the failure data to generate repair solutions for
activating certain of the redundant rows and columns for each of the plurality of
semiconductor devices.